COURSE DETAIL

VLSI SYSTEM TESTING
Country Taiwan
Host Institution National Taiwan University
Program(s) National Taiwan University
UCEAP Course Level Upper Division
UCEAP Subject Area(s) Electrical Engineering
UCEAP Course Number 102
UCEAP Course Suffix
UCEAP Official Title VLSI SYSTEM TESTING
UCEAP Transcript Title VLSI SYSTEM TEST
UCEAP Quarter Units 4.50
UCEAP Semester Units 3.00

Course Description

With the advancement in Integrated Circuit (IC) fabrication and integration technologies, design-for-test and system-level testing have become indispensable. This course discusses concepts and technologies in VLSI testing. It starts with fault modeling, fault simulation, and test pattern generation. Then, the course introduces design-for-test, built-in-self-test, and memory testing. Finally, the course will address challenges and solutions to system-level tests.

Language(s) of Instruction
English

Host Institution Course Number
EEE5011

Host Institution Course Title
VLSI SYSTEM TESTING

Host Institution Campus

Host Institution Faculty
College of Electrical Engineering and Computer Science

Host Institution Degree

Host Institution Department
Graduate Institute of Electrical Engineering

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